20220-96590T

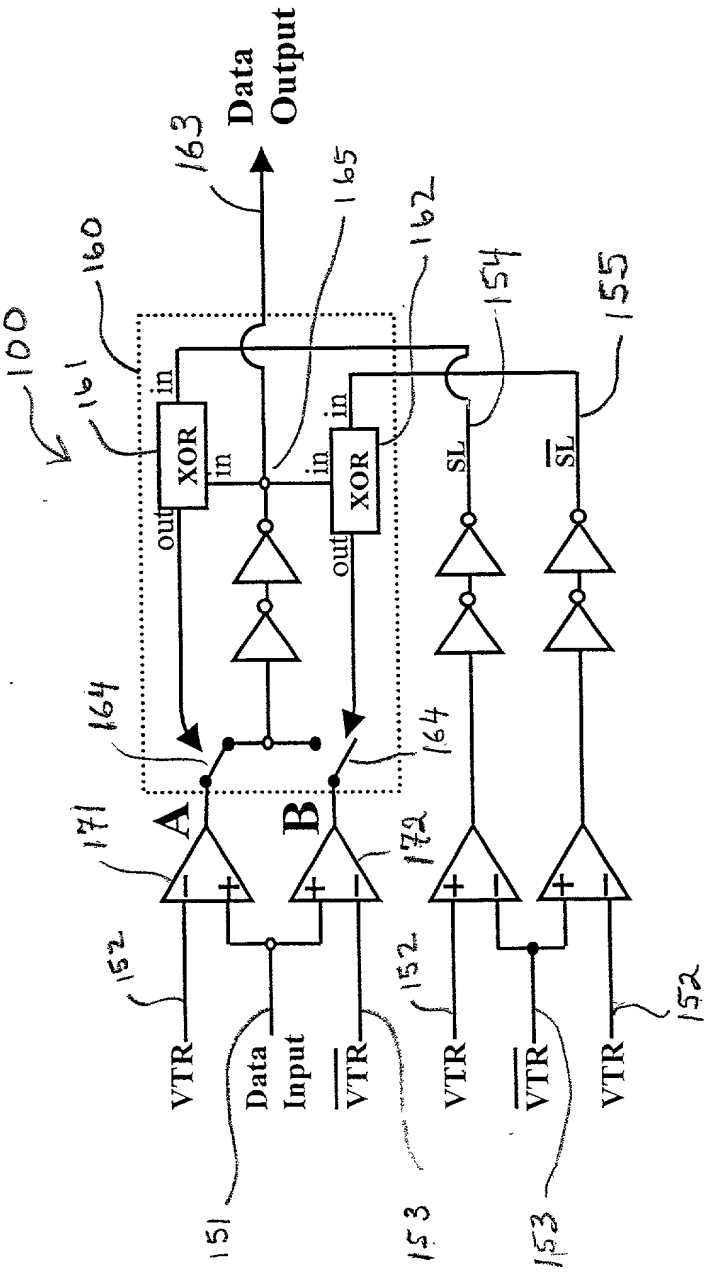


FIG. 1A

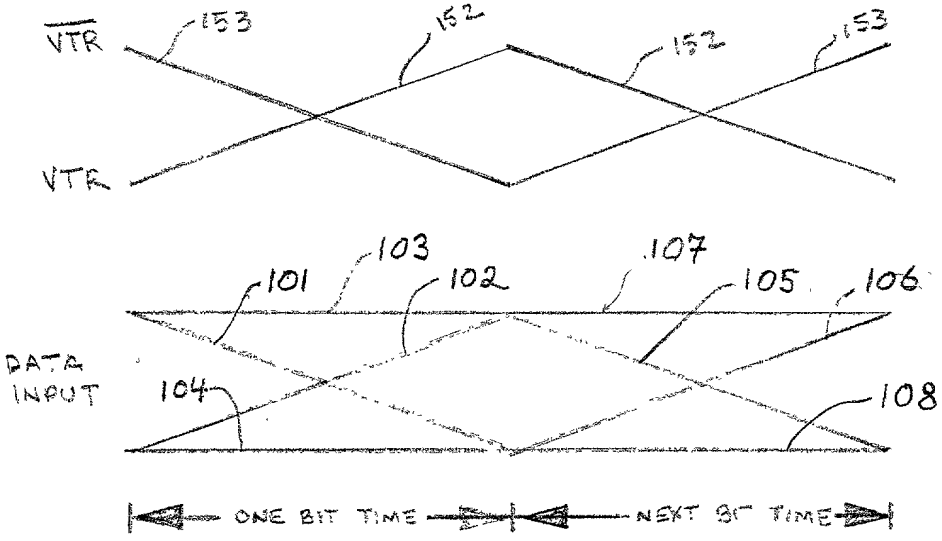


FIG. 1B

30,720,465,900

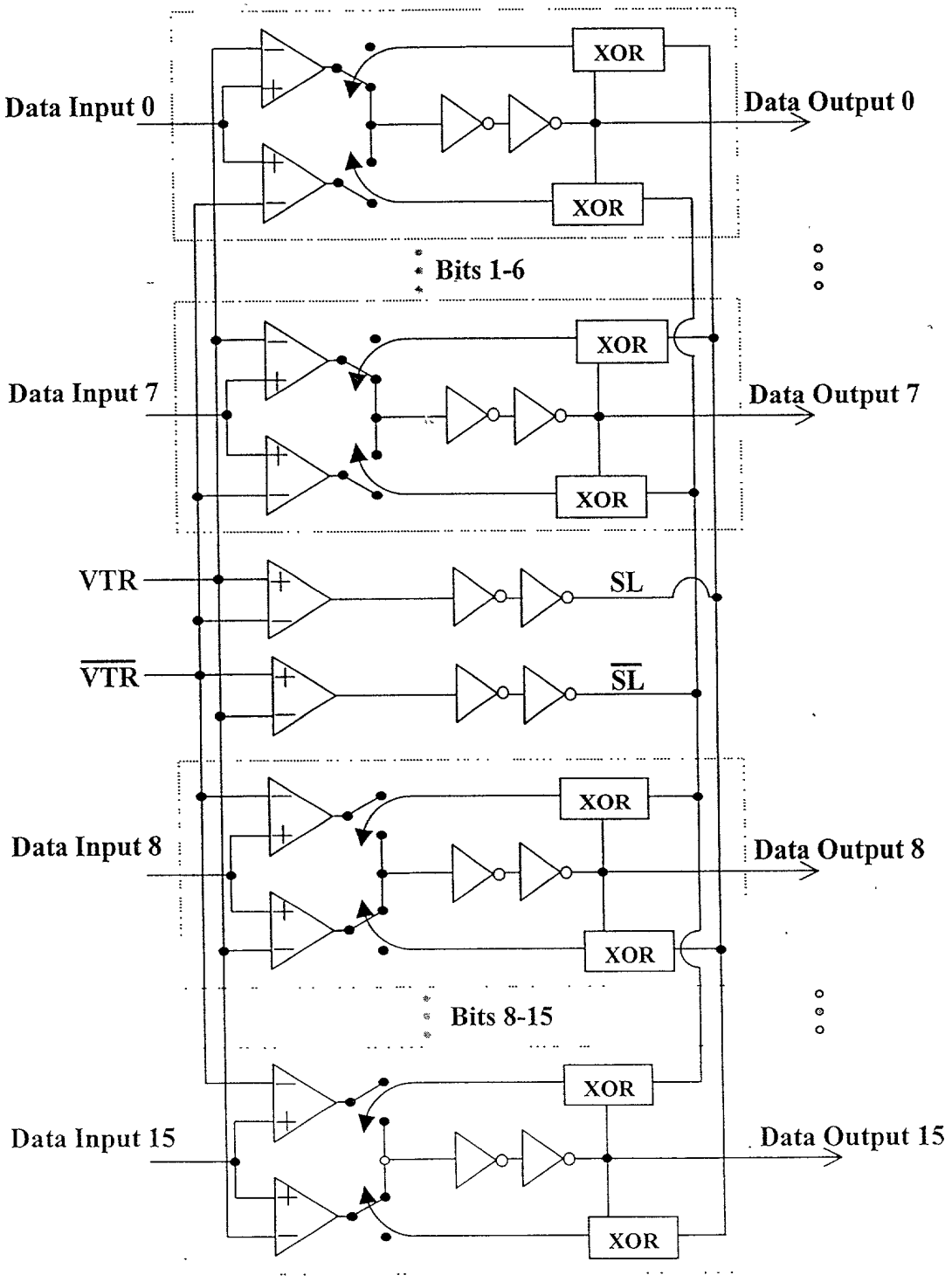


FIG. 2

20220 "05 960 0T

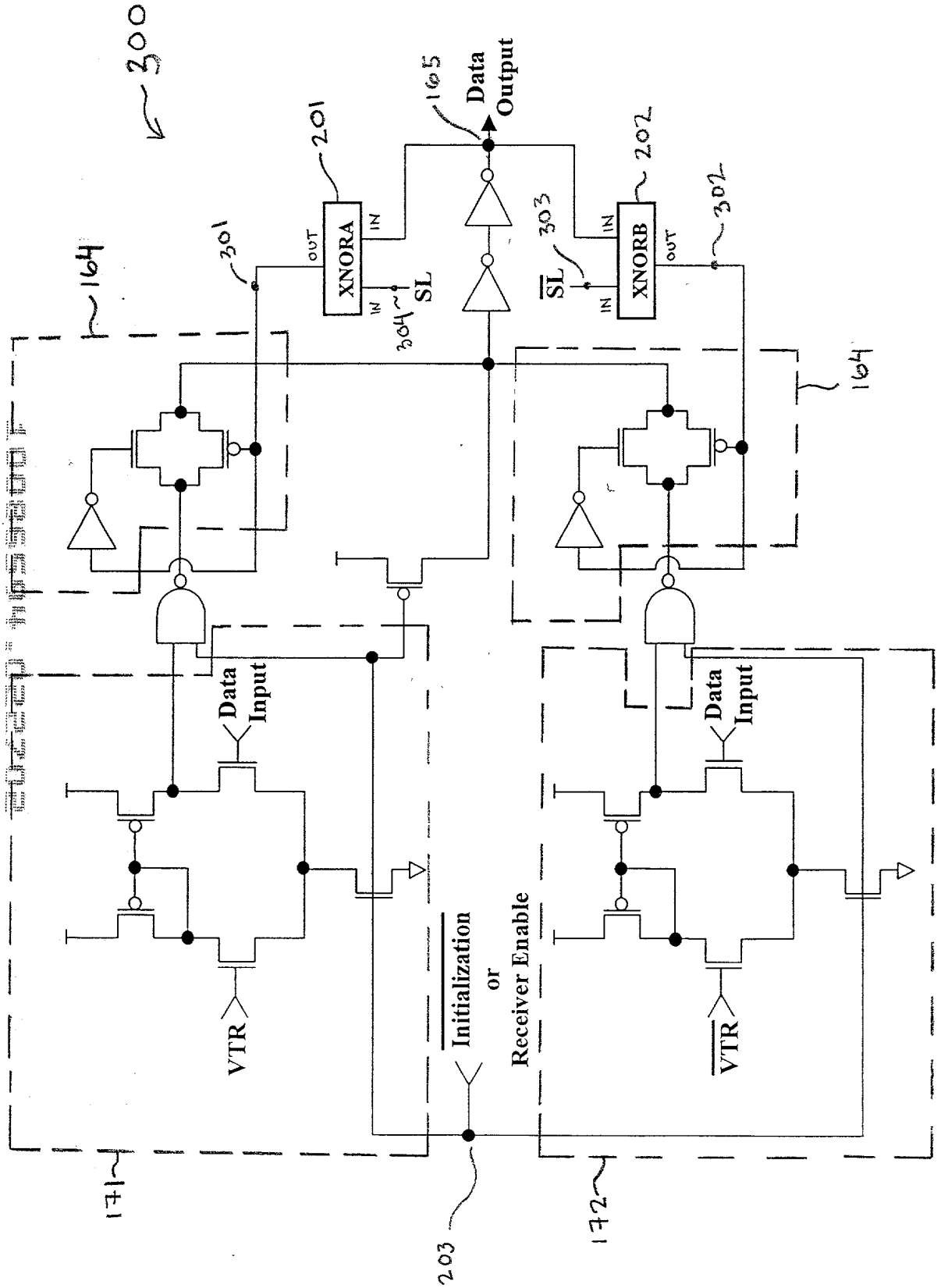

300
201
202
165
Data Output
XNORA
XNORB
IN
OUT
SL
$\overline{SL}$
301
302
303
304
164
Data Input
VTR
$\overline{VTR}$
$\overline{\text{Initialization}}$ or Receiver Enable
171
172
203

FIG. 3

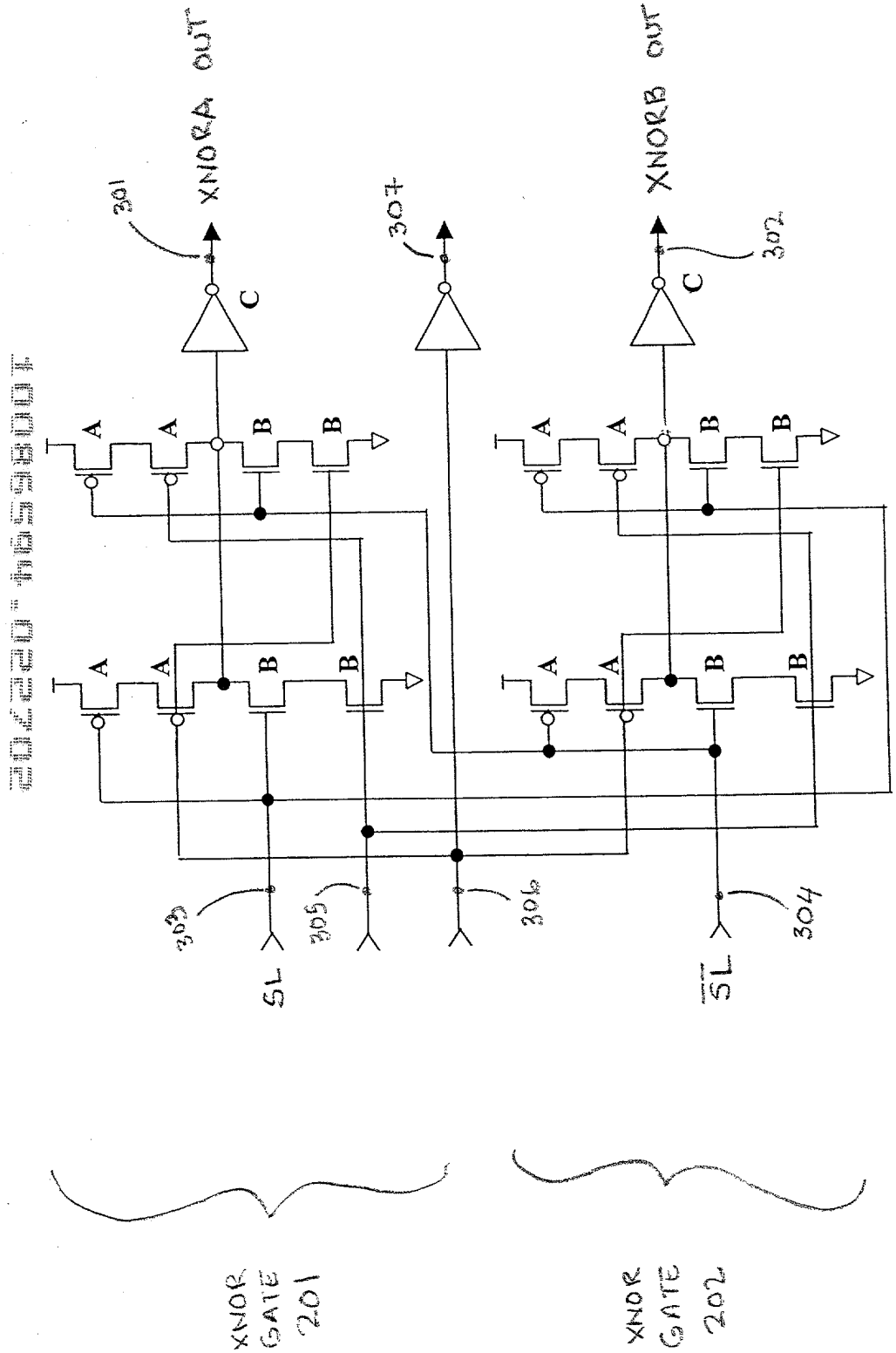

XNORA OUT
XNORB OUT
301
307
302
C
A
B
303
305
306
304
SL
$\overline{SL}$
XNOR GATE 201
XNOR GATE 202

FIG. 4

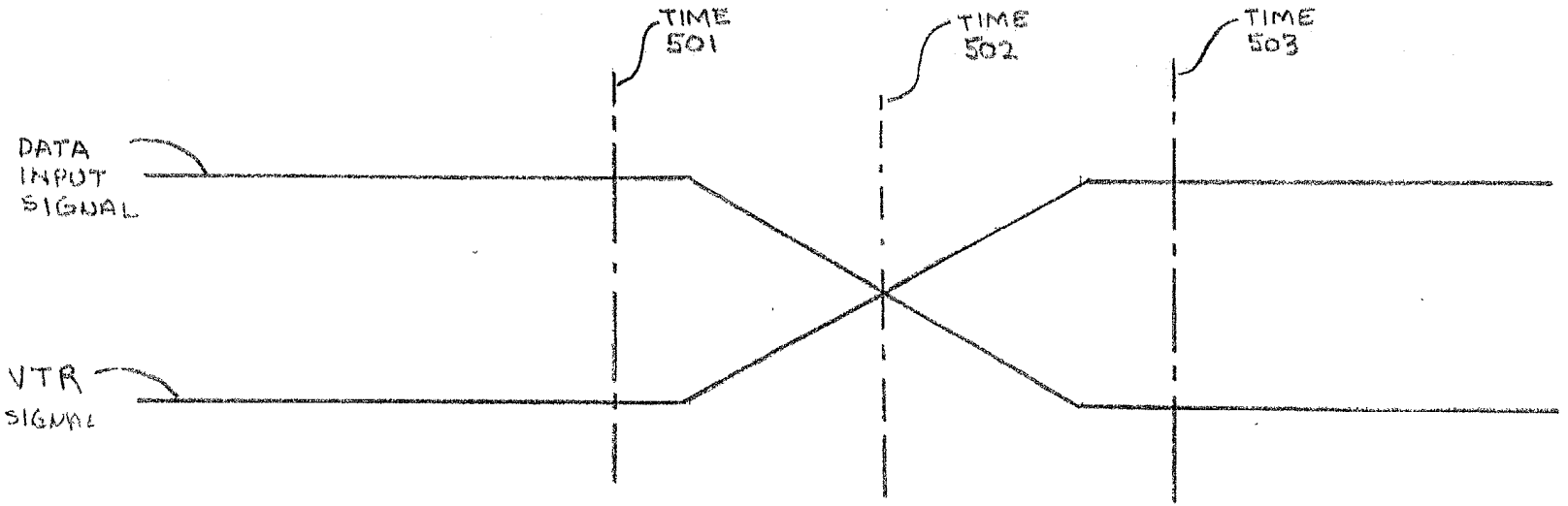

TIME
501
TIME
502
TIME
503
DATA
INPUT
SIGNAL
VTR
SIGNAL

FIG. 5A

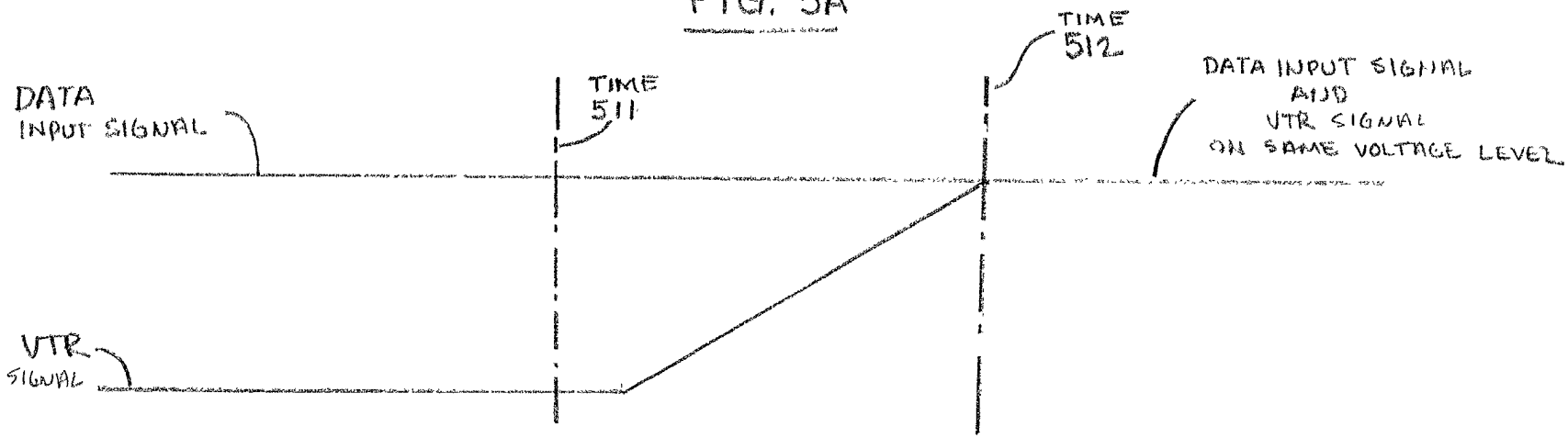

TIME
512
DATA INPUT SIGNAL
AND
VTR SIGNAL
ON SAME VOLTAGE LEVEL
TIME
511
DATA
INPUT SIGNAL
VTR
SIGNAL

FIG. 5B

3d220 "06590T

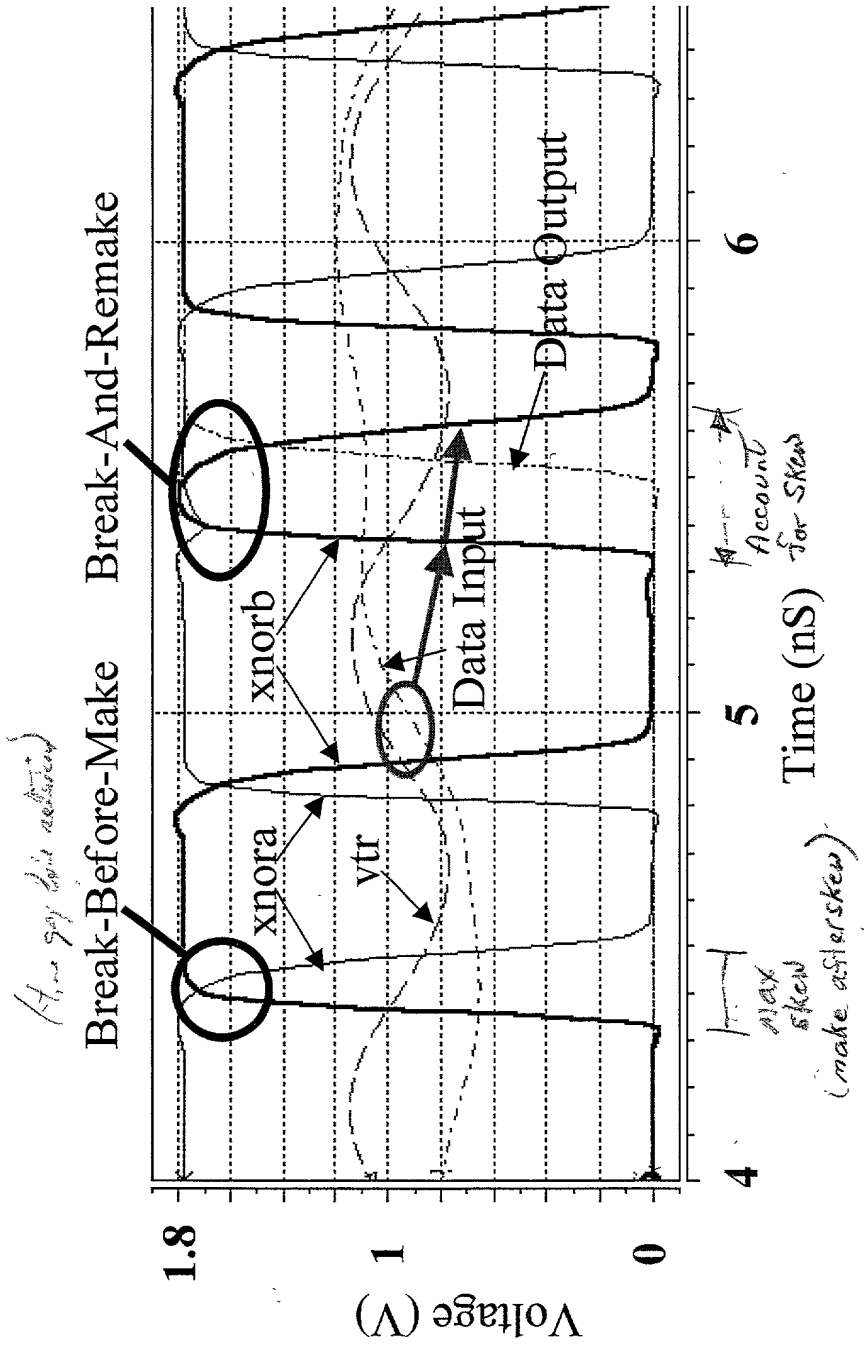


FIG. 5C
(Replacing XOR with XNOR)

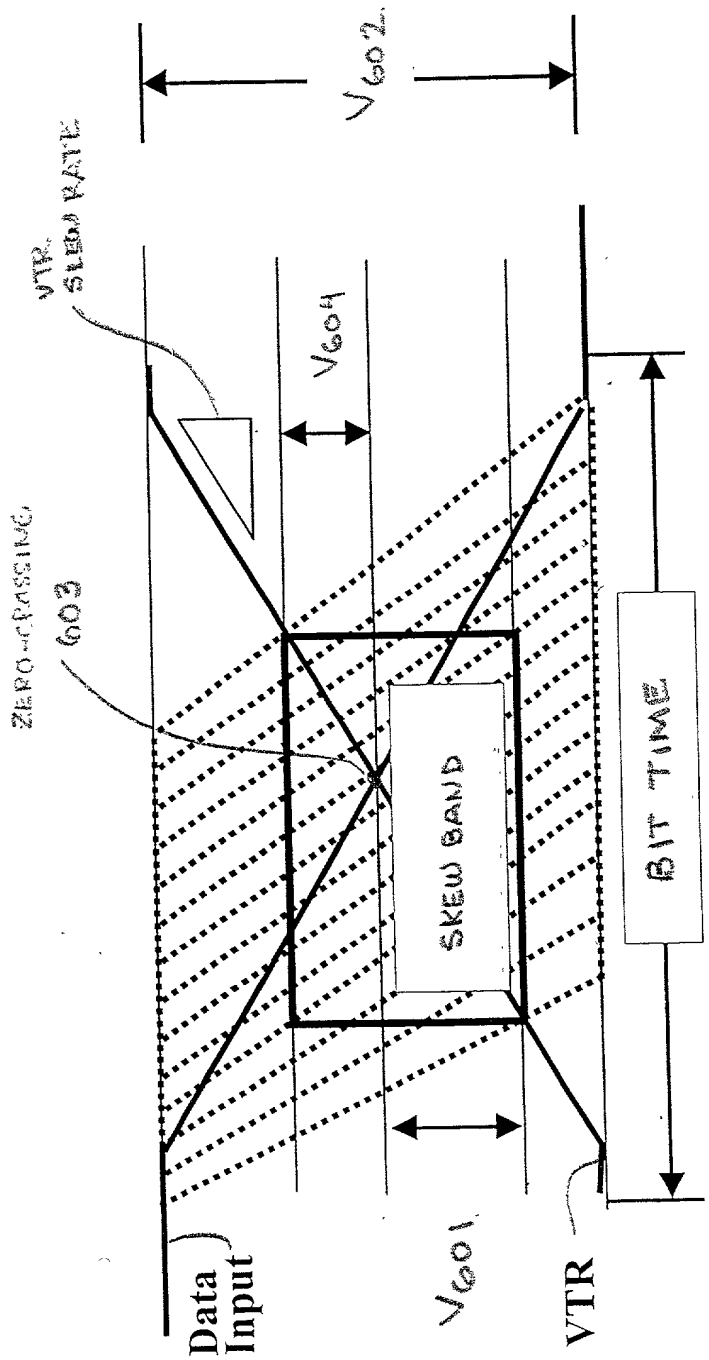


FIG. 6

20220405.1659800E

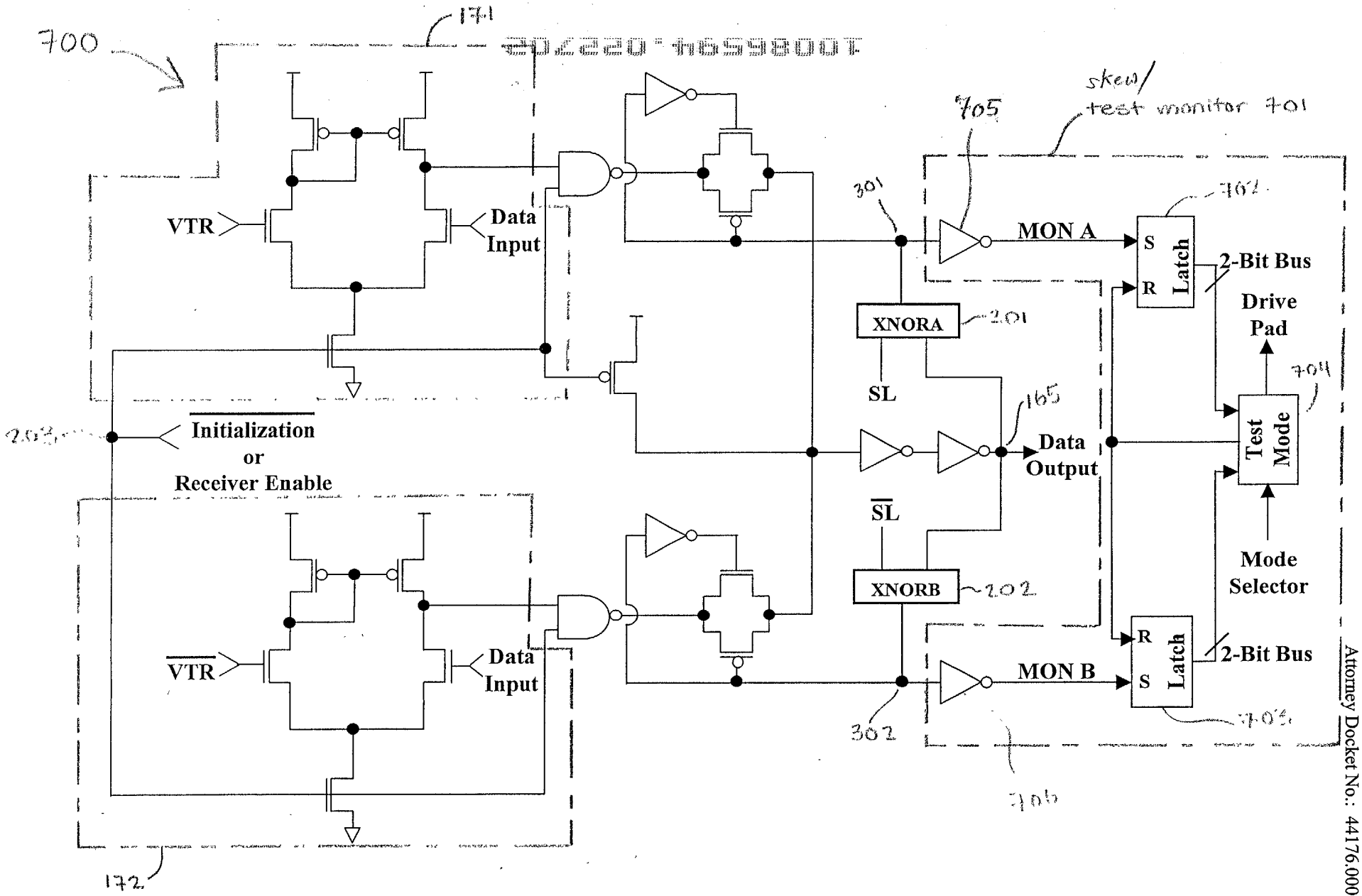


FIG. 7A

METHOD AND SYSTEM FOR DESKEWING PARALLEL BUS CHANNELS TO INCREASE DATA TRANSFER RATES
Inventors: Ejaz Ul Haq, et al.
Attorney Docket No.: 44176.00036

20020201.1659

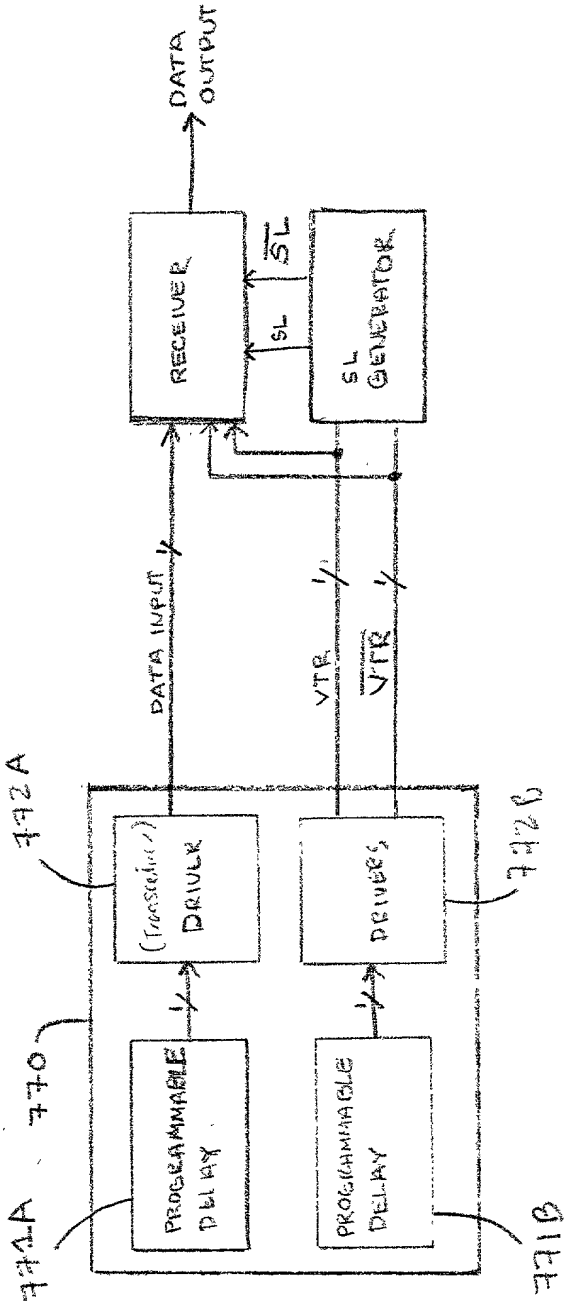
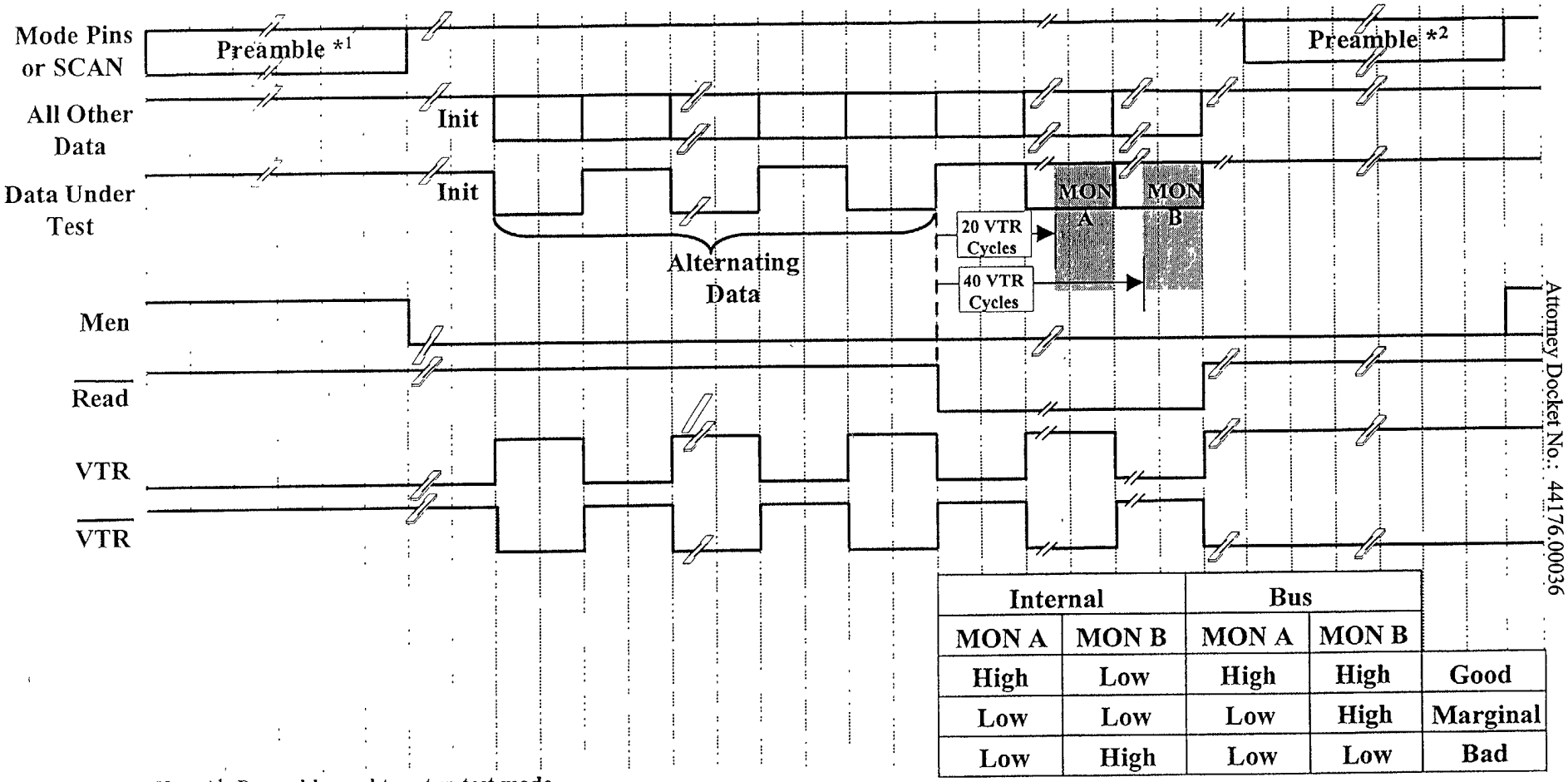


FIG. 7B



Internal		Bus		
MON A	MON B	MON A	MON B	
High	Low	High	High	Good
Low	Low	Low	High	Marginal
Low	High	Low	Low	Bad

Note *1: Preamble used to setup test mode

Note *2: Preamble used to setup next test mode, terminate test mode or set registers

FIG. 8A

20220 "A659800F

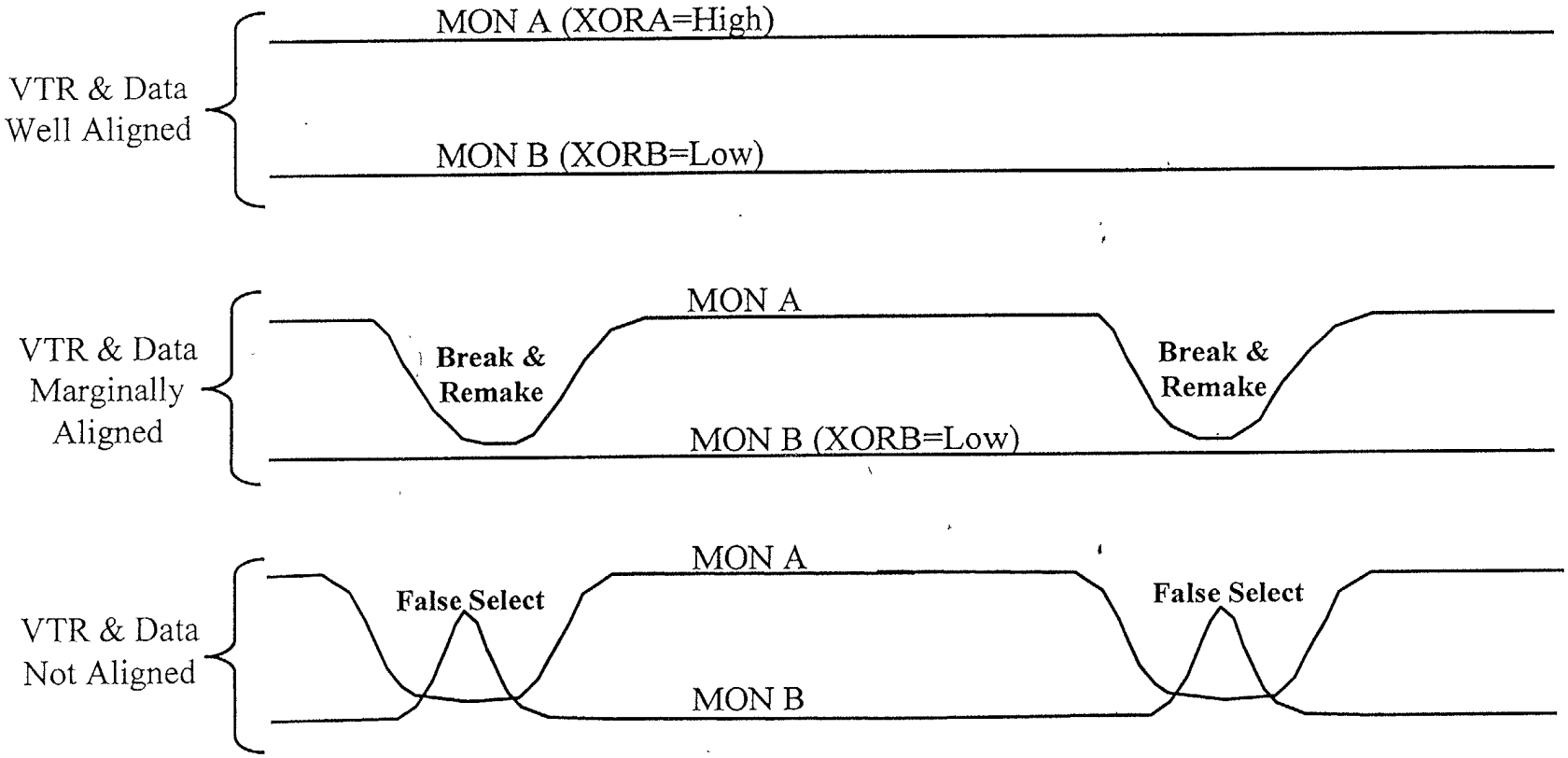


FIG. 8B

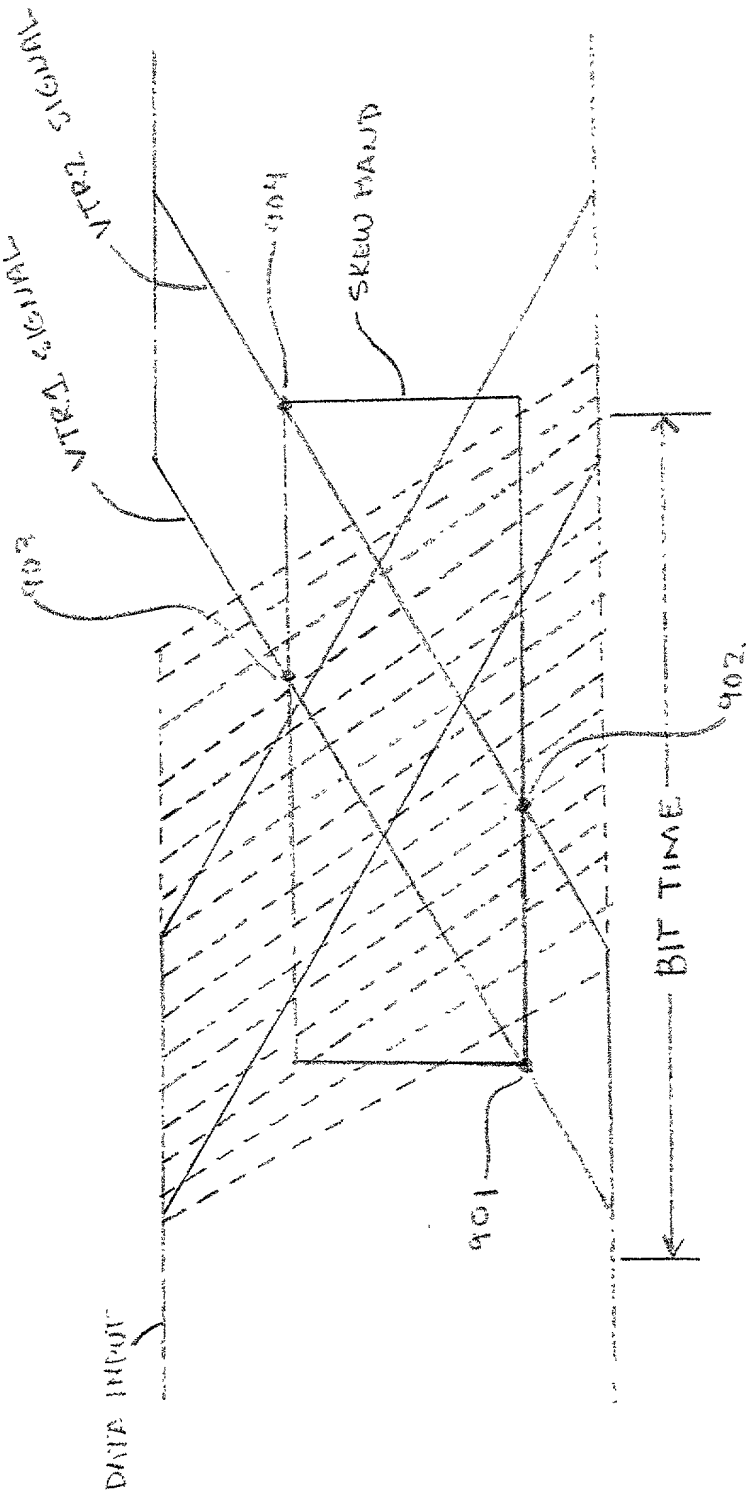


FIG. 9

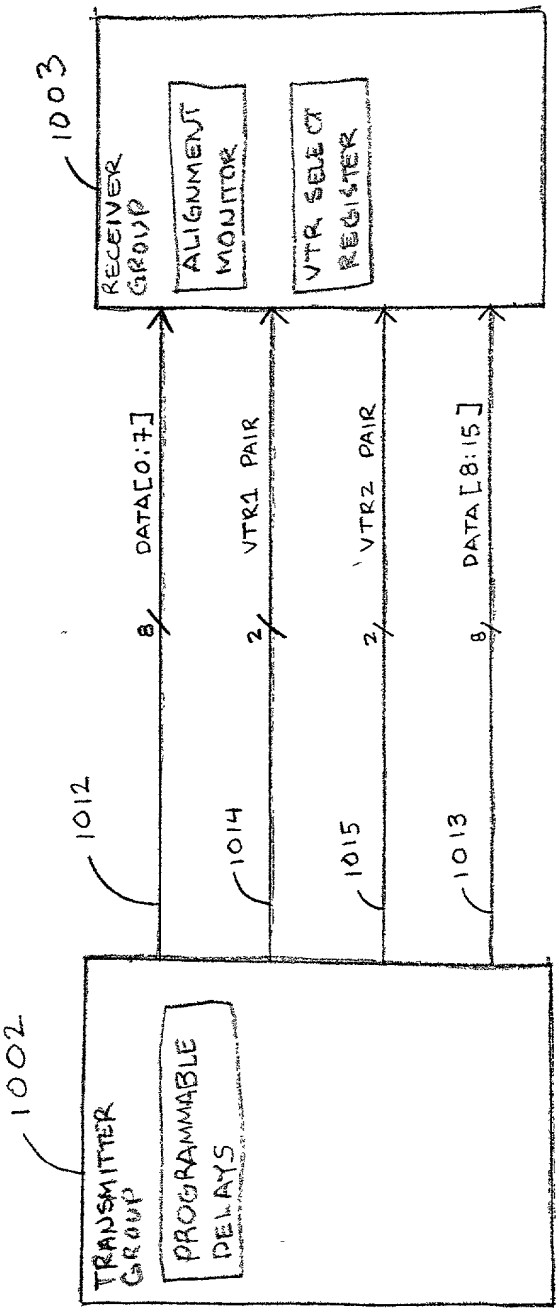

1003
RECEIVER GROUP
ALIGNMENT MONITOR
VTR SELECT REGISTER
1012
1014
1015
1013
8
DATA[0:7]
2
VTR1 PAIR
2
VTR2 PAIR
8
DATA[8:15]
1002
TRANSMITTER GROUP
PROGRAMMABLE DELAYS

FIG. 10

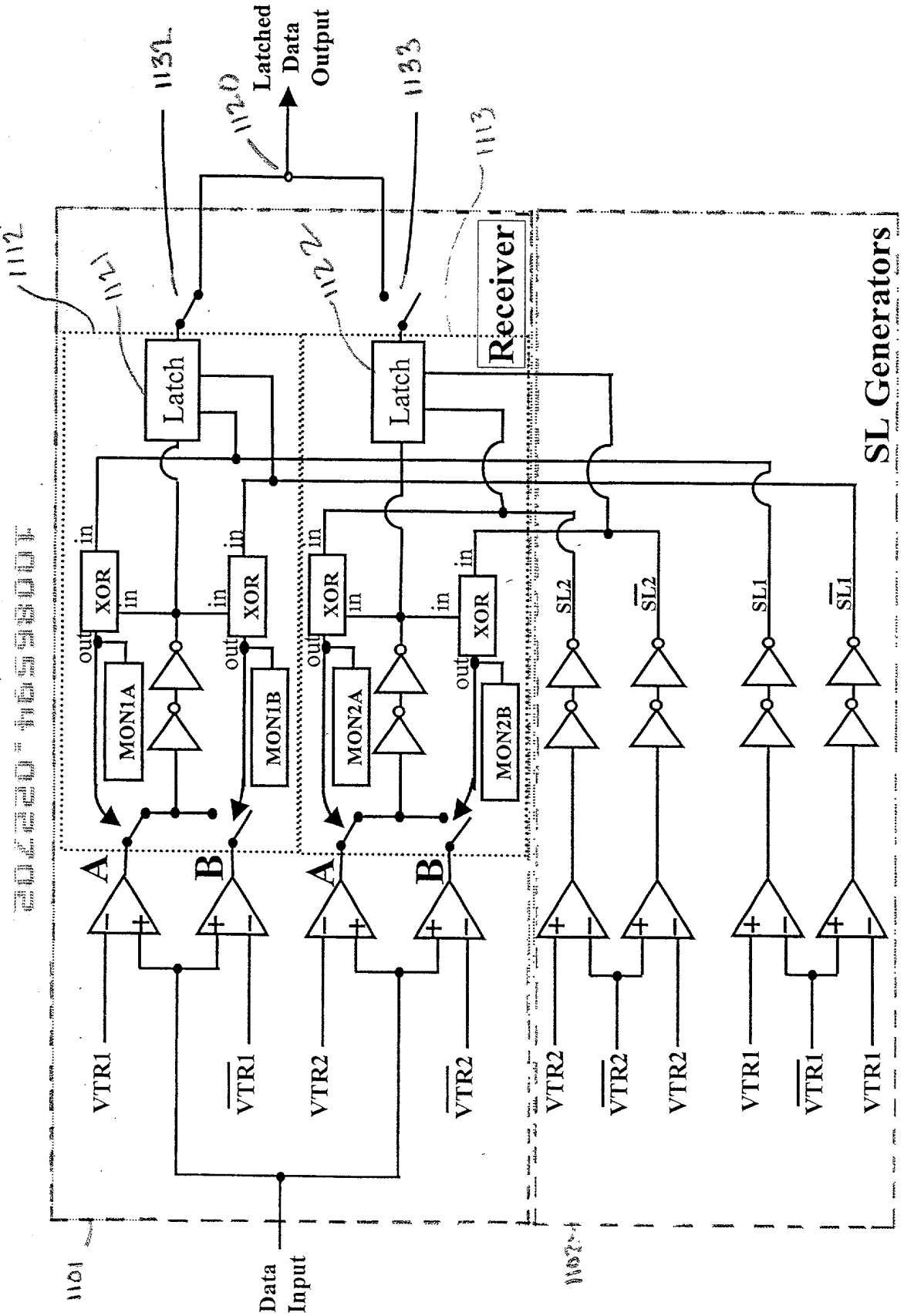

1131
1120
Latched Data Output
1133
1112
1121
1122
1113
Receiver
Latch
Latch
SL Generators
in
XOR
out
MON1A
MON1B
MON2A
MON2B
SL2
SL2
SL1
SL1
A
B
VTR1
VTR1
VTR2
VTR2
VTR2
VTR2
VTR1
VTR1
VTR1
1101
Data Input

FIG. 11

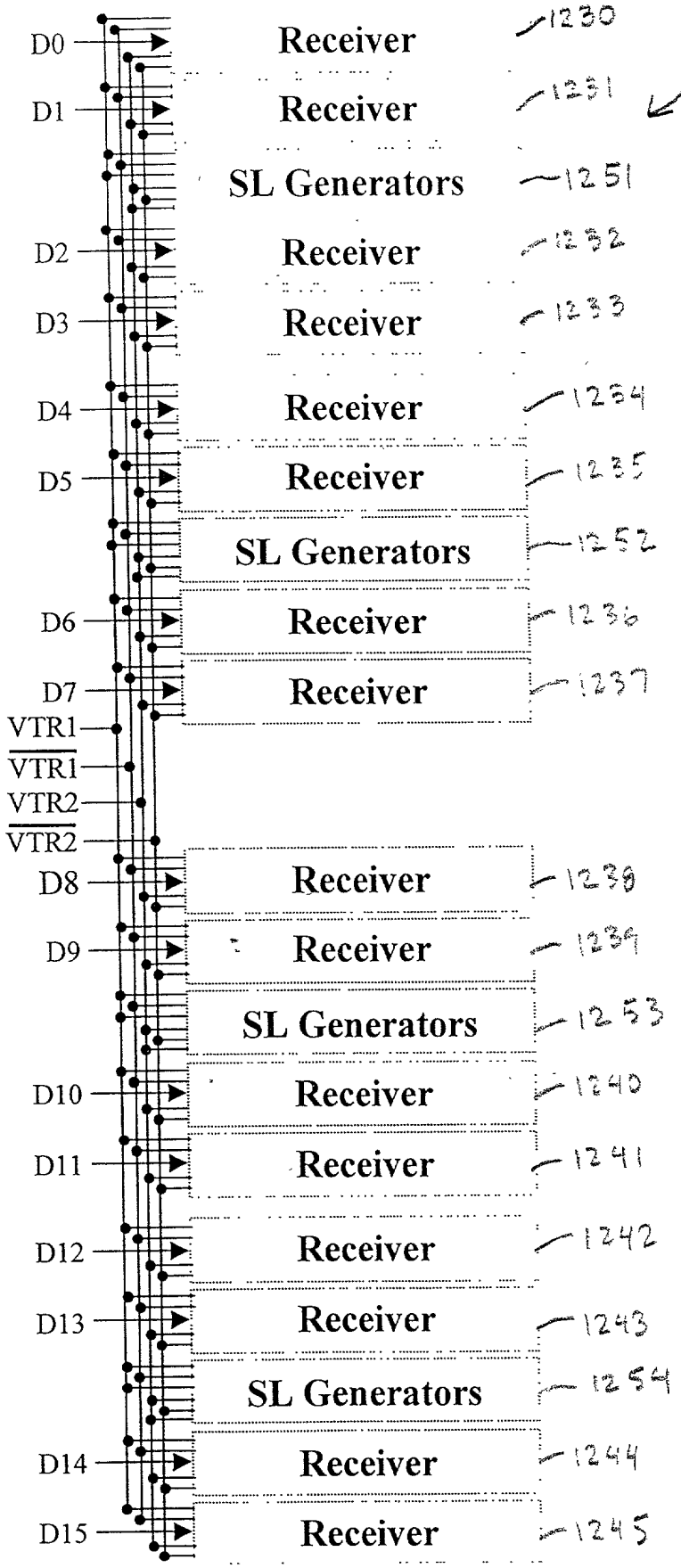
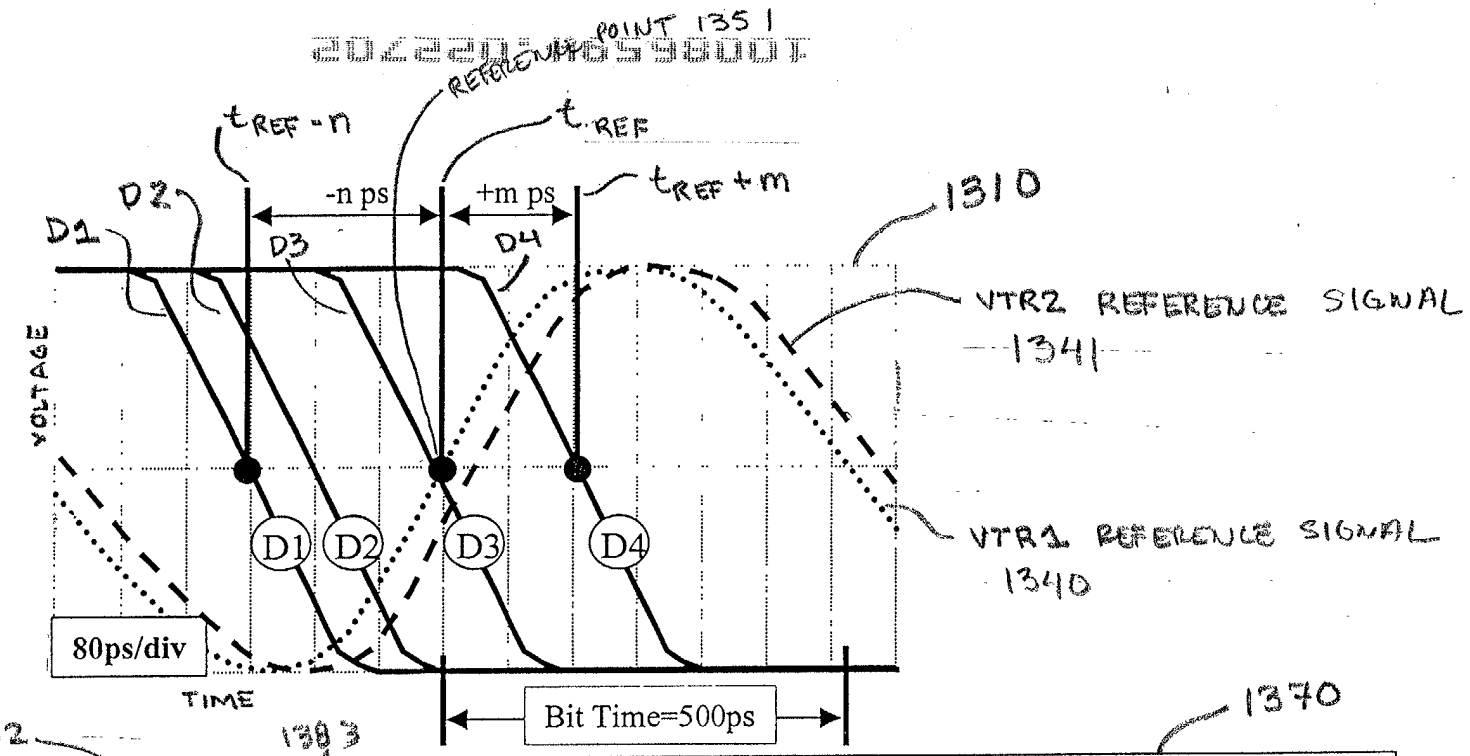


FIG. 12

Docket #44176.00036



1370

	Results											
VTR2=VTR1+40ps	D1-80ps	D1	D1+80ps	D2-80ps	D2	D2+80ps	D3-80ps	D3	D3+80ps	D4-80ps	D4	D4+80ps
VTR1 REF -160 PS		Pass	Pass	Pass	Pass	Pass	Pass					
VTR2 REF -160 PS		Pass	Pass	Pass	Pass	Pass	Pass					
VTR1 REF -80PS			Pass		Pass	Pass	Pass	Pass				
VTR2 REF -80 PS			Pass		Pass	Pass	Pass	Pass				
VTR1 REF						Pass	Pass	Pass	Pass	Pass		
VTR2 REF						Pass	Pass	Pass	Pass	Pass		
VTR1 REF +80 PS								Pass	Pass	Pass	Pass	
VTR2 REF +80 PS								Pass	Pass	Pass	Pass	
VTR1 REF +160 PS									Pass	Pass	Pass	Pass
VTR2 REF +160 PS									Pass	Pass	Pass	Pass

1381 1382 1383 1391 1392 1371 1372 1373 1374

FIG. 13

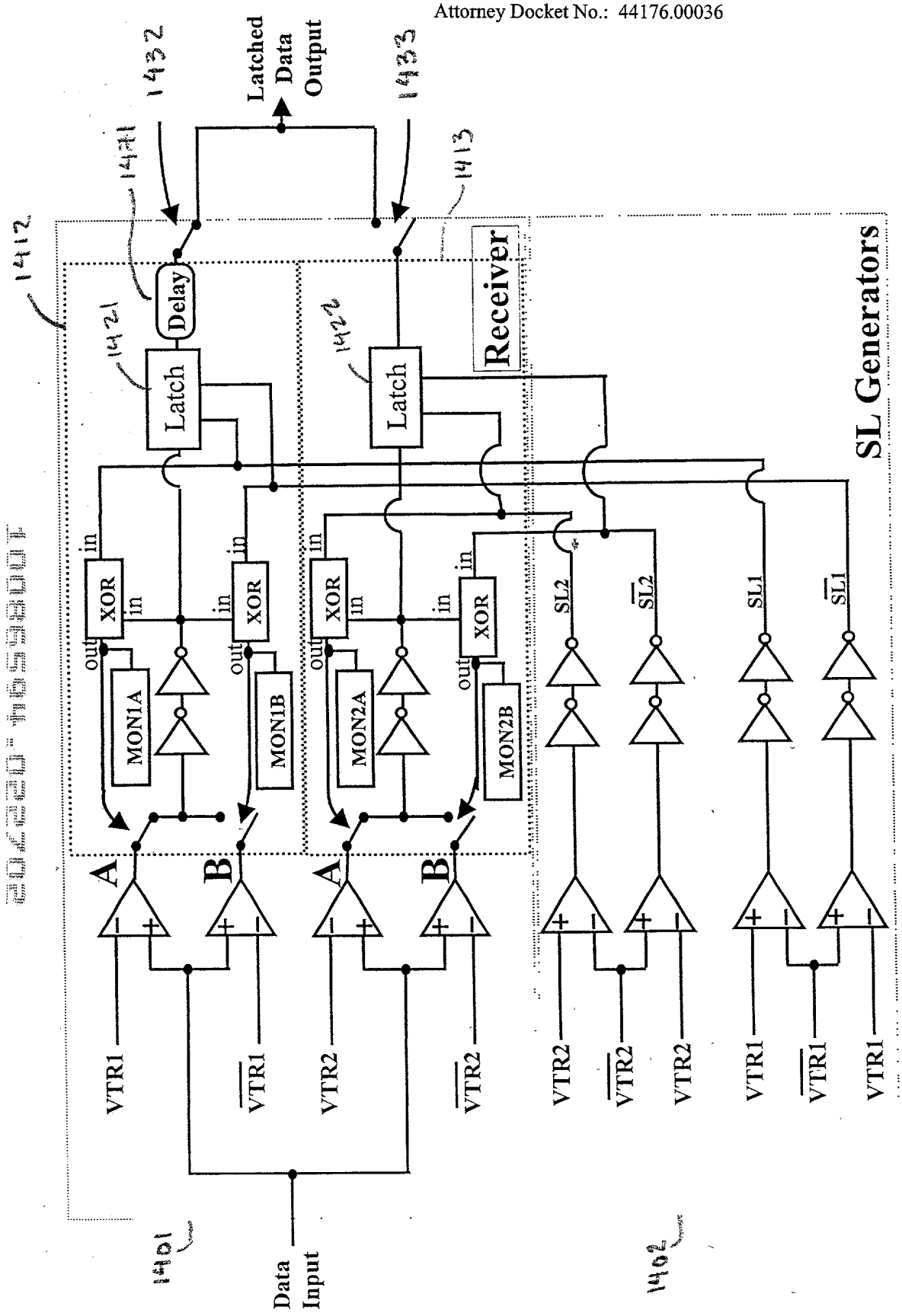

1412
1432
Latched Data Output
1433
1431
1413
Delay
Receiver
1421
1422
Latch
Latch
SL Generators
in
XOR
out
MON1A
MON1B
MON2A
MON2B
A
B
SL2
$\overline{SL2}$
SL1
$\overline{SL1}$
VTR1
$\overline{VTR1}$
VTR2
$\overline{VTR2}$
Data Input
1401
1402

FIG. 14

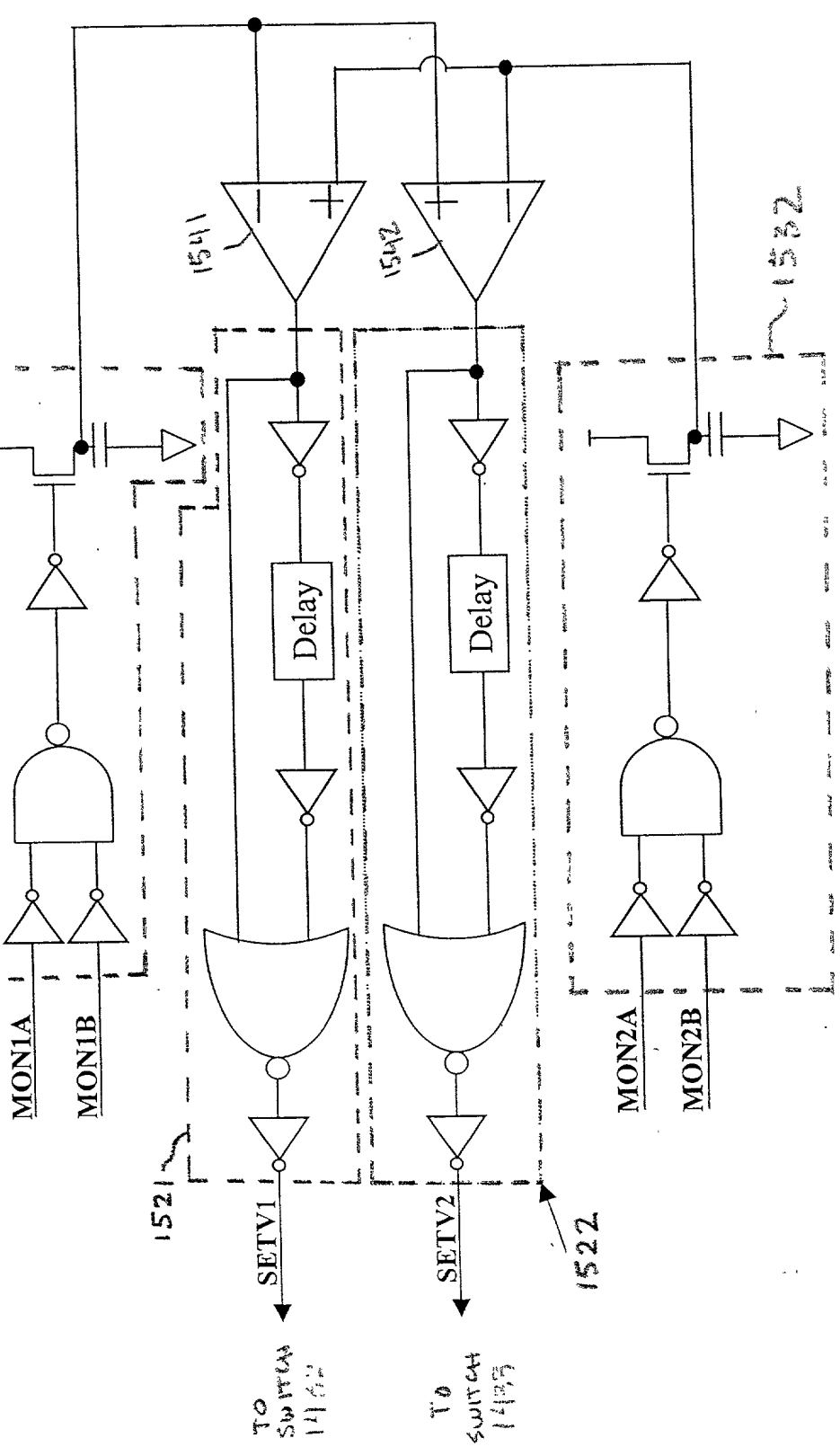

1501
1511
1512
1532
1531
Delay
Delay
MON1A
MON1B
MON2A
MON2B
1521
1522
SETV1
SETV2
To Switch 1425
To Switch 1425

FIG. 15